

FIG. 1

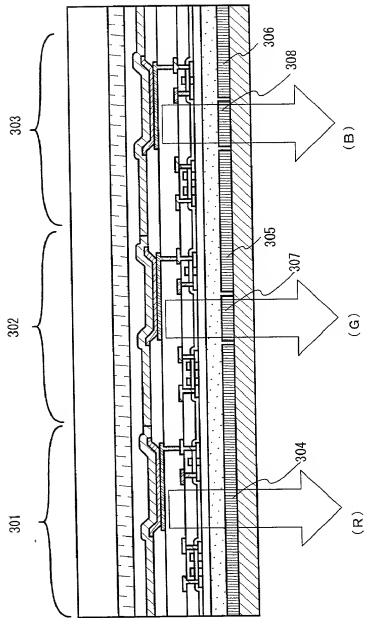


FIG. 2

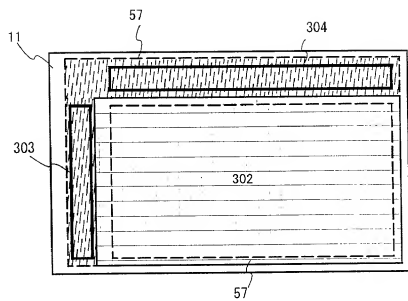
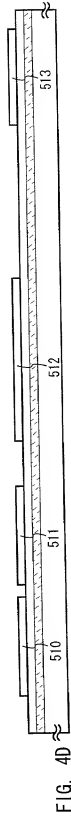
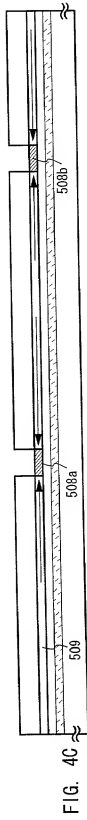
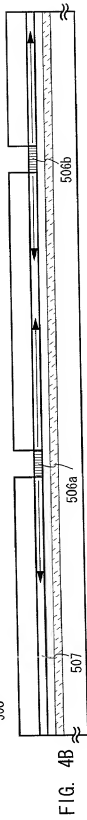
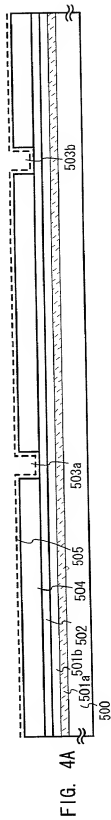


FIG. 3



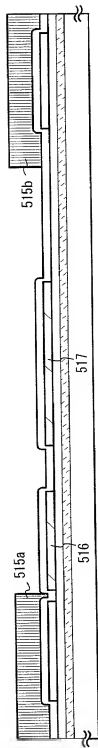


FIG. 5A

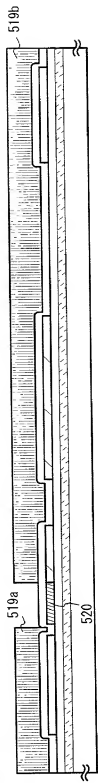


FIG. 5B

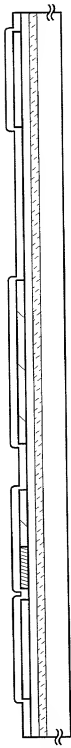


FIG. 5C

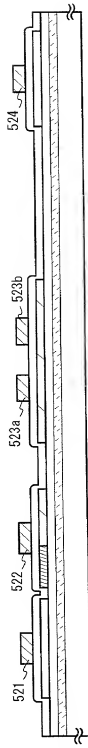


FIG. 5D

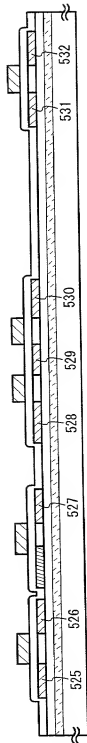


FIG. 6A

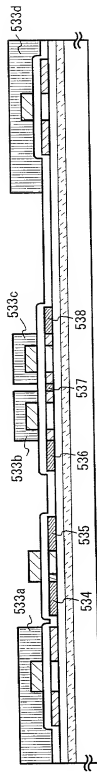


FIG. 6B

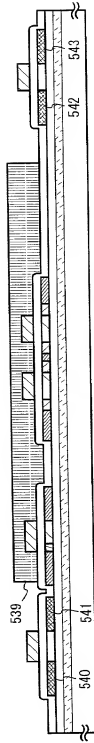


FIG. 6C

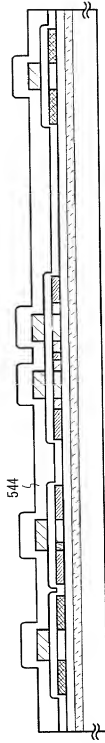


FIG. 6D

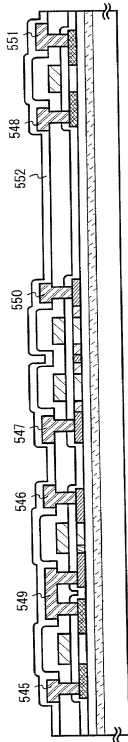


FIG. 7A

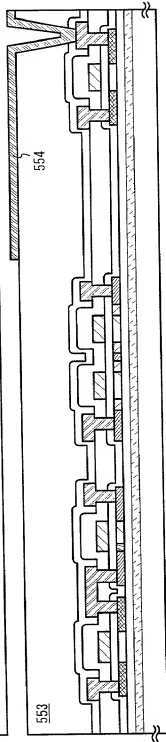


FIG. 7B

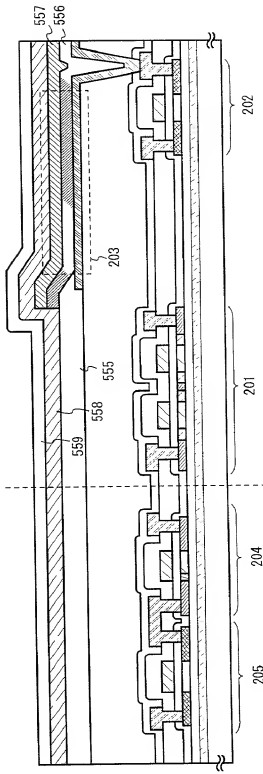


FIG. 7C

FIG. 8A

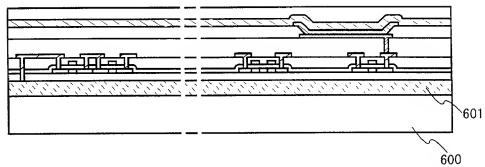


FIG. 8B

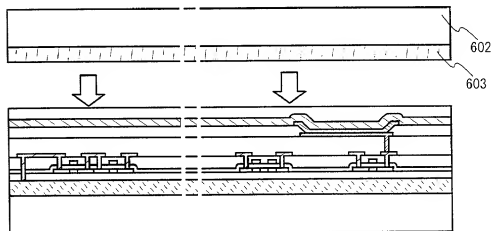
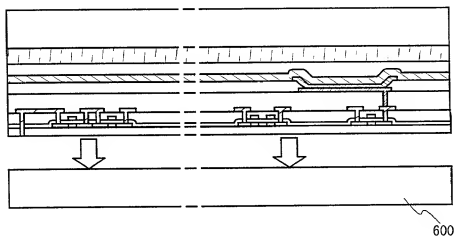


FIG. 8C



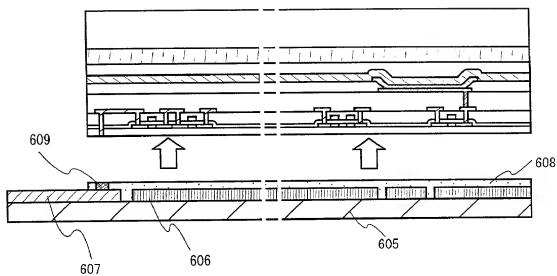


FIG. 9A

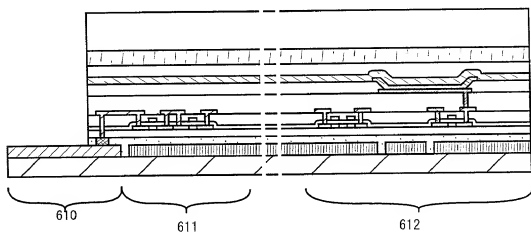


FIG. 9B

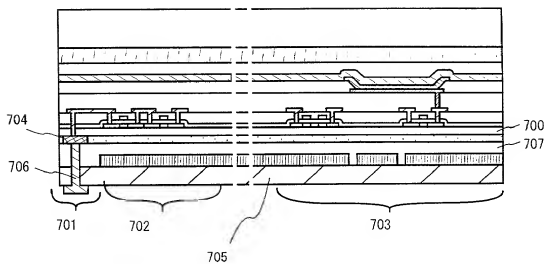


FIG. 10A

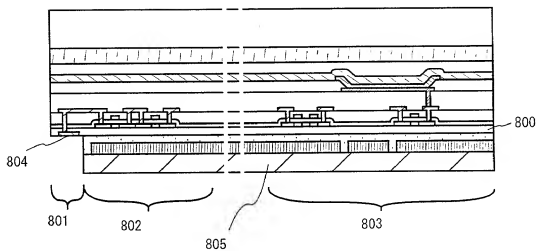


FIG. 10B

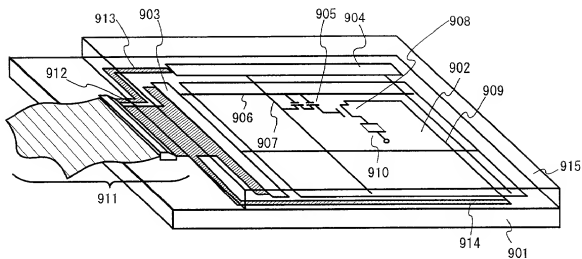


FIG. 11

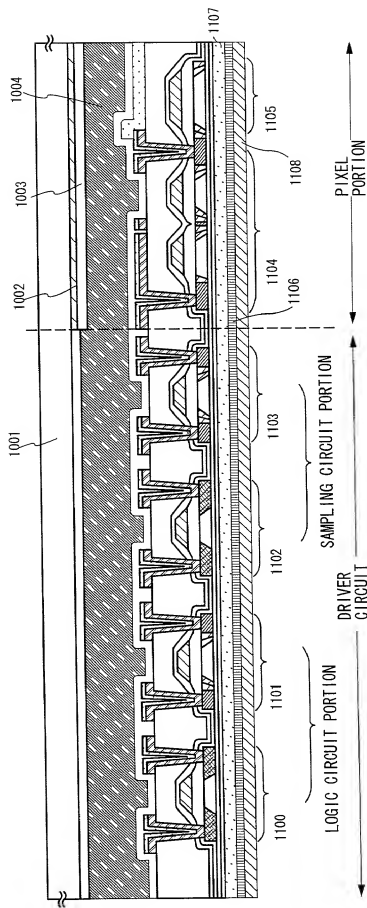


FIG. 12

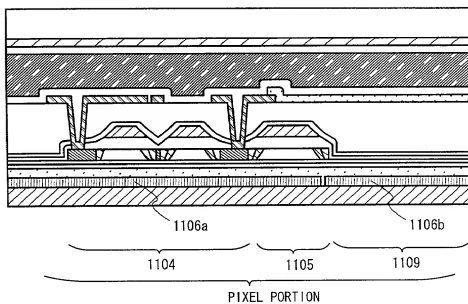


FIG. 13

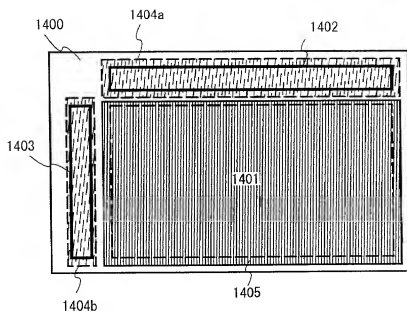


FIG. 14A

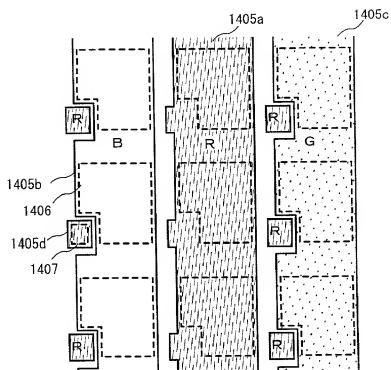


FIG. 14B

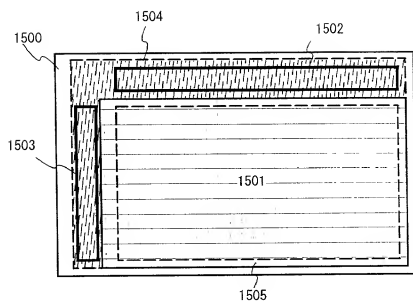


FIG. 15A

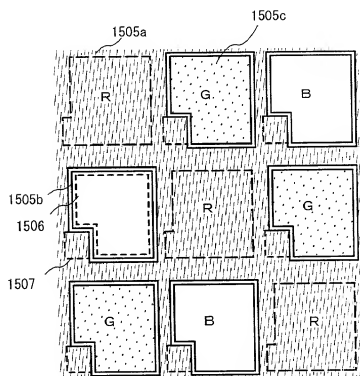


FIG. 15B

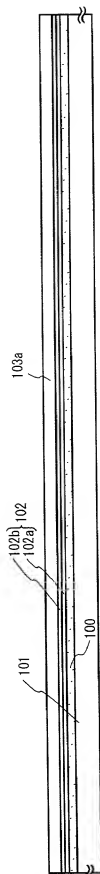


FIG. 16A

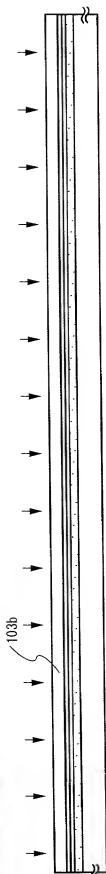


FIG. 16B

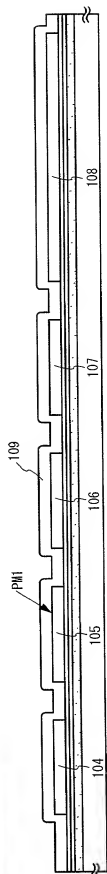


FIG. 16C

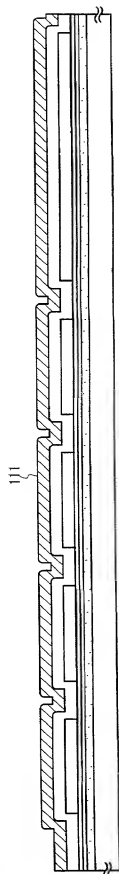


FIG. 16D

This cross-sectional view illustrates a pixel circuit structure divided into three functional regions: the Logic Circuit Portion, the Sampling Circuit Portion, and the Pixel Portion. The structure is built upon a substrate 159.

- Logic Circuit Portion:** This region contains the first two PMOS transistors, PM1 and PM2. PM1 (160a, 160b, 165a, 165b) and PM2 (161a, 161b, 162a, 162b) are connected to a common source 166a and a common gate 166b. PM2 is also connected to a common drain 167a. PM3 (163a, 163b) and PM4 (164a, 164b) are connected to a common source 163b and a common gate 164a. PM4 is also connected to a common drain 167b. The gates of PM1 and PM2 are connected to a common gate line 207c, while the gates of PM3 and PM4 are connected to a common gate line 207b.
- Sampling Circuit Portion:** This region contains the third PMOS transistor, PM5 (215a, 215b, 216a, 216b), and the first NMOS transistor, NM1 (210, 213a, 213b, 213c). PM5 and NM1 are connected to a common source 212 and a common gate 211c. PM5 is also connected to a common drain 214a. NM1 is connected to a common drain 210 and a common gate 211a. The gates of PM5 and NM1 are connected to a common gate line 211b, while the gates of PM3 and PM4 are connected to a common gate line 211a.
- Pixel Portion:** This region contains the second NMOS transistor, NM2 (217, 214b, 218, 219a, 219b), and the second PMOS transistor, PM6 (225, 226, 227, 228). NM2 and PM6 are connected to a common source 217 and a common gate 218. NM2 is also connected to a common drain 214b. PM6 is connected to a common drain 225 and a common gate 226. The gates of NM2 and PM6 are connected to a common gate line 227, while the gates of PM5 and NM1 are connected to a common gate line 228.

The structure is completed with a common drain 225 and a common gate 226. The gates of PM5 and NM1 are connected to a common gate line 211b, while the gates of PM3 and PM4 are connected to a common gate line 211a.

FIG. 18B

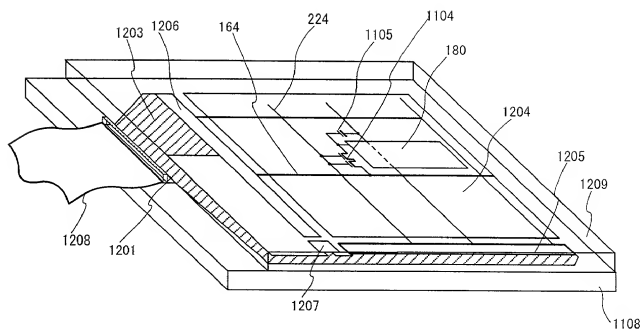


FIG. 19

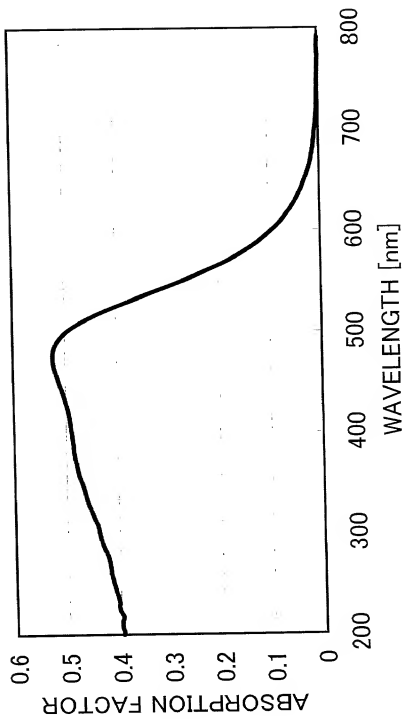


FIG. 20

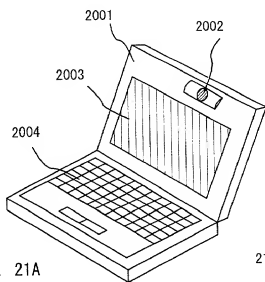


FIG. 21A

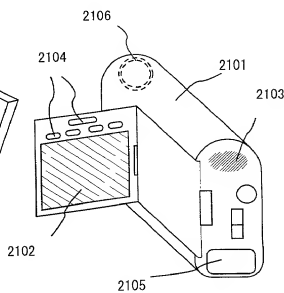


FIG. 21B

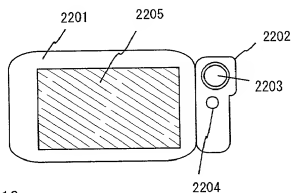


FIG. 21C

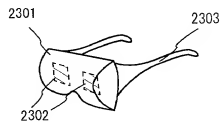


FIG. 21D

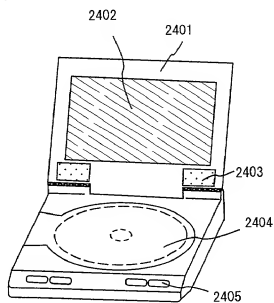


FIG. 21E

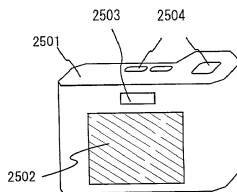


FIG. 21F

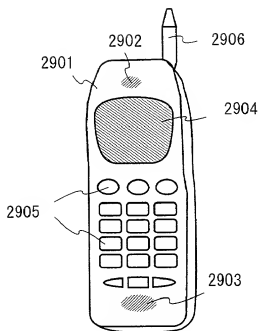


FIG. 22A

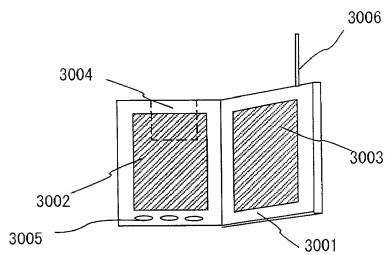


FIG. 22B

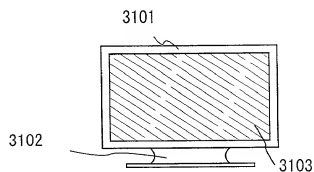


FIG. 22C